CLAIMS

What is claimed is:

1. An apparatus comprising:

a clock generator, distributed over an integrated circuit, including a plurality of cells each coupled to multiple adjacent ones of said plurality of cells by different clock wires, wherein, for each of said plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge.

2. The apparatus of claim 1, wherein the clock generator is distributed in two dimensions over the integrated circuit.

3. The apparatus of claim 1, wherein the clock generator is distributed in three dimensions over the integrated circuit.

4. The apparatus of claim 1, wherein current travels in one direction on each of the clock wires.

5. The apparatus of claim 1, wherein each of the plurality of cells to detect a plurality of clock edges being currently generated by said clock generator and trigger a next clock edge based on arrival times of the detected plurality of clock edges.

6. The apparatus of claim 1, wherein each of different parts of synchronous logic is coupled through one or more amplifiers to a different one of the clock wires of said clock generator.

7. The apparatus of claim 1, wherein different parts of synchronous logic are coupled to different ones of the clock wires of said clock generator, and wherein said different parts of the synchronous logic are interconnected.

8. The apparatus of claim 1, wherein the integrated circuit is one of a square and a rectangle.

9. The apparatus of claim 1, wherein the integrated circuit is of an irregular shape.

10. The apparatus of claim 1 wherein said clock generator uses asynchronous type detection techniques to determine when to trigger a next clock edge to provide a synchronous time reference for synchronous logic distributed over the integrated circuit.

11. An apparatus comprising:

a clock generator to generate a clock signal through the interaction of a plurality of cells distributed in grid over an integrated circuit, wherein each of said plurality of cells is coupled to multiple adjacent complementary ones of said plurality of cells by different clock wires; and

a plurality of sets of synchronous logic each coupled to a different one of the clock wires, wherein said plurality of sets of synchronous logic are interconnected.

12. The apparatus of claim 11, wherein the grid is two-dimensional.

13. The apparatus of claim 11, wherein the gird is three-dimensional.

14. The apparatus of claim 11, wherein current travels in one direction on the clock wires.

15. The apparatus of claim 11, wherein each of said plurality of cells is to detect clock edges being currently generated by the adjacent complementary ones of said plurality of cells and to trigger a next clock edge based on arrival times of the detected clock edges.

16. The apparatus of claim 11, wherein said clock generator is a closed loop system.

17. The apparatus of claim 11, wherein each of said plurality of cells receives clock signals generated by adjacent complementary ones of said plurality of cells and synchronizes the next clock edge based thereon.

18. The apparatus of claim 11, wherein at least some of the plurality of cells and the clock wires are routed on the integrated circuit in proximity to the power supply routing on the integrated circuit. .

19. The apparatus of claim 11, wherein certain of said plurality of cells are pull-up type cells and others of said plurality of cells are pull-down type cells.

20. The apparatus of claim 19, wherein at least said pull-up type cells or said pull-down type cells include initialization circuitry.

21. An integrated circuit including:

a clock generator including a plurality of cells distributed in grid over an integrated circuit that collectively form an oscillator of said clock generator, wherein each of the plurality of cells oscillate dependent upon clock signals received from multiple of others of the plurality of cells; and

a plurality of sets of synchronous logic, distributed over said integrated circuit, coupled to be clocked by said clock generator.

22. The apparatus of claim 21, wherein the grid is two-dimensional.

23. The apparatus of claim 21, wherein the gird is three-dimensional.

24. The apparatus of claim 21, wherein each of said plurality of cells is to detect clock edges from the received clock signals and to trigger a next clock edge based on arrival times of the detected clock edges.

25. The apparatus of claim 21, wherein said clock generator is a closed loop system.

26. The apparatus of claim 21, wherein said plurality of cells, based upon arrival times of clock edges of the clock signals received, synchronizes the next clock edge.

27. The apparatus of claim 21, wherein at least some of the plurality of cells are routed on the integrated circuit in proximity to positive supply of the integrated circuit.

28. The apparatus of claim 21, wherein at least some of the plurality of cells are routed on the integrated circuit in proximity to negative supply of the integrated circuit.

29. The apparatus of claim 21, wherein at least some of the plurality of cells are routed on the integrated circuit in between positive and negative supply of the integrated circuit.

30. An integrated circuit comprising:

a distributed clock generator including,

a plurality of cells that, responsive to an averaging of a previous clock edge produced by said plurality of cells, detect when to produce the next clock edge, and

a plurality of clock wires each coupling together two of said plurality of cells such that said plurality of cells are coupled together in grid; and

a plurality of sets state holding elements each having a clock input, each clock input of each of said sets coupled to a different one of said plurality of clock wires.

31. The apparatus of claim 30, wherein the grid is two-dimensional.

32. The apparatus of claim 30, wherein the gird is three-dimensional.

33. The integrated circuit of claim 30, wherein, on any one of said plurality of clock wires, the current always travels in the same direction once the clock signal has be initialized.

34. The integrated circuit of claim 30, wherein said clock inputs are coupled to said clock wires through a set of one or more serially coupled inverters.

35. The apparatus of claim 30, wherein said distributed clock generator is a closed loop system.

36. The apparatus of claim 30, wherein at least some of the plurality of cells and clock wires are routed on the integrated circuit in proximity to positive supply of the integrated circuit.

37. The apparatus of claim 30, wherein at least some of the plurality of cells and clock wires are routed on the integrated circuit in proximity to negative supply of the integrated circuit.

38. The apparatus of claim 30, wherein at least some of the plurality of cells and clock wires are routed on the integrated circuit between positive and negative supply of the integrated circuit.

39. A distributed clock generator comprising:
a plurality of cells each including,
a plurality of terminals,
a cumulative clock edge detection circuit coupled to said plurality of terminals and having an output,
a delay/amplification circuit coupled to said output of said cumulative clock edge detection circuit, and
a driver circuit coupled to said plurality of terminals and to said delay/amplification circuit;
a plurality of clock wires, each of said plurality of clock wires coupling one of said plurality of terminals of one of said plurality of cells to one of said plurality of terminals of another of said plurality of cells.

40. The distributed clock generator of claim 39, wherein the plurality of cells are distributed in two dimensions.

41. The distributed clock generator of claim 39, wherein the plurality of cells are distributed in three dimensions.

42. The distributed clock generator of claim 39, wherein current travels in one direction on the plurality of clock wires.

43. The apparatus of claim 39, wherein at least some of the plurality of cells and the plurality of clock wires are routed on an integrated circuit in proximity to the power supply routing on the integrated circuit.

44. The distributed clock generator of claim 39, wherein each of said plurality of cells is either a pull-up type cell or a pull-down type cell, and each of said plurality of clock wires couples one of said plurality of terminals of one of said pull-up type cells to one of said plurality of terminals of one of said pull-down type cells.

45. The distributed clock generator of claim 39, wherein each of said plurality of cells is a hybrid type cell in which each driver circuit includes at least one pull-up driver and at least one pull-down driver coupled to different ones of said plurality of terminals, and wherein said plurality of clock wires couple together the terminals coupled to pull-up drivers and pull-down drivers.

46. The distributed clock generator of claim 39, wherein each of said cumulative clock edge detection circuits phase mix clock signals received on said plurality of terminals.

47. The distributed clock generator of claim 39, wherein each of the cumulative clock edge detection circuits includes:

a plurality of transistors each having a gate, a source, and a drain, each of the gates of said plurality of transistors of said cumulative clock edge detection circuit are coupled to a different one of said plurality of terminals, the drains of said plurality of transistors of said cumulative clock edge detection circuit are coupled to together to form a node to provide said output, and the sources of said plurality of transistors of said cumulative clock edge detection circuit are coupled some to positive and others to negative supply.

48. The distributed clock generator of claim 39, wherein each of the cumulative clock edge detection circuits includes:

a plurality of inverters each having an input and output, each of the inputs of said plurality of inverters of said cumulative clock edge detection circuit are coupled to a different one of said plurality of terminals, the outputs of said plurality of inverters of said cumulative clock edge detection circuit are coupled to together to form a node to provide said output.

49. The distributed clock generator of claim 39, wherein each of the driver circuits includes:

a plurality of transistors each having a gate, a source, and a drain, each of the drains of said plurality of transistors of said driver circuit are coupled to a different one of said plurality of terminals, the gates of said plurality of

transistors of said driver circuit are shorted together, and the sources of said plurality of transistors of said driver circuit are coupled to either positive or negative supply.

50. The distributed clock generator of claim 49, wherein the sources of said plurality of transistors of some of said driver circuits are coupled to positive supply, and the sources of said plurality of transistors of others said driver circuits are coupled to negative supply.

51. The distributed clock generator of claim 49, wherein the sources of said plurality of transistors of each of said driver circuit are coupled some to positive and others to negative supply.

52. An integrated circuit comprising:

a distributed clock generator including a plurality of cells collectively having a plurality of terminal pairs, each of said plurality of terminal pairs including a charging terminal coupled to a discharging terminal to have generated therebetween a clock signal having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal, the terminals of each of said plurality of terminal pairs being part of two different ones of said plurality of cells, said plurality of cells coupled together as a result of each being coupled to certain others of said plurality of cells by said plurality of terminal pairs; and

a plurality of sets of synchronous logic each having a clock input, each clock input of each of said sets coupled to receive the clock signal of one of said plurality of terminal pairs.

53. The distributed clock generator of claim 52, wherein the plurality of cells are distributed in two dimensions.

54. The distributed clock generator of claim 52, wherein the plurality of cells are distributed in three dimensions.

55. The distributed clock generator of claim 52, wherein current travels in one direction between each of said plurality of terminal pairs.

56. The apparatus of claim 52, wherein at least some of the plurality of cells and their interconnection by said plurality of terminal pairs are routed on an integrated circuit in proximity to the power supply routing on the integrated circuit.

57. The distributed clock generator of claim 52, wherein each of said plurality of cells includes either multiple of the charging terminals or multiple of the discharging terminals of said plurality of terminal pairs.

58. The distributed clock generator of claim 52, wherein each of said plurality of cells includes both multiple of the charging terminals and the discharging terminals of said plurality of terminal pairs.

59. The distributed clock generator of claim 52, each of said plurality of cells to phase mix clock signals received on said plurality of terminals.

60. The cell of claim 59, wherein, for each of said plurality of cells, the phase mix is an average phase when the difference in the arrival times of the clock edges of said clock signals on its terminals are within a period of time roughly equivalent to the rise/fall of the clock signal.

61. The cell of claim 59, wherein, for each of said plurality of cells, the phase mix is a non-linear function of the phases of said clock signals on its terminals.

62. A cell of a distributed clock generator comprising:

a set of terminals of said cell, each of said terminals in said set being one terminal of a different terminal pair, each of said terminal pairs including a charging terminal coupled to a discharging terminal to have generated therebetween a clock signal having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal;

a cumulative clock edge detection circuit coupled to said set of terminals to determine a single clock edge transition time reflective of transitions of said clock signals on said terminals,

a driver circuit coupled to said set of terminals; and

a delay/amplification circuit, coupled to an output of said cumulative clock edge detection circuit and to said driver circuit, to cause another clock edge transition of said clock signals to substantially simultaneously occur some delay time after each of said single clock edge transition times.

63. The cell of claim 62, wherein the set of terminals of said cell are charging terminals.

64. The cell of claim 62, wherein the set of terminals of said cell are discharging terminals.

65. The cell of claim 62, wherein the set of terminals of said cell including both charging and discharging terminals.

66. The cell of claim 62, wherein said cumulative clock edge detection circuit includes:

a plurality of transistors each having a gate, a source, and a drain, each of the gates of said plurality of transistors of said cumulative clock edge detection circuit are coupled to a different one of said set of terminals, the drains of said plurality of transistors of said cumulative clock edge detection circuit are coupled to together to form a node, and the sources of said plurality of transistors of said cumulative clock edge detection circuit are coupled some to positive and others to negative supply.

67. The cell of claim 62, wherein said driver circuit includes:

a plurality of transistors each having a gate, a source, and a drain, each of the drains of said plurality of transistors of said driver circuit are coupled to a different one of said set of terminals, the gates of said plurality of transistors of said driver circuit are shorted together, and the sources of said plurality of transistors of said driver circuit are coupled to either positive or negative supply.

68. The cell of claim 67, wherein the sources of said plurality of transistors said driver circuit are coupled to positive supply.

69. The cell of claim 67, wherein the sources of said plurality of transistors of said driver circuits are coupled to negative supply.

70. The cell of claim 67, wherein the sources of said plurality of transistors of said driver circuit are coupled some to positive and others to negative supply.

71. The cell of claim 62, wherein said cumulative clock edge detection circuit to determine said single clock edges transition time based on an average phase when the difference in the arrival times of the clock edges of said clock signals on said terminals are within a period of time roughly equivalent to the rise/fall of the clock signal.

72. The cell of claim 62, wherein said cumulative clock edge detection circuit to determine said single clock edges transition time as a non-linear function of the phases of said clock signals on said terminals.

73. The cell of claim 62, wherein said cumulative clock edge detection circuit includes smaller transistors than transistors in said driver circuit.

74. The cell of claim 62, wherein the delay time is tunable using variable delay inverters.

75. A method for generating a clock in a distributed manner, said method comprising:

each of a plurality of cells, coupled to adjacent others of said plurality of cells to

receive clock signals, performing the following,

determining a moment in time based upon the arrival times of current clock edges of received clock signals;

delaying a period of time after said moment in time; and

triggering a next clock edge to said adjacent others of said plurality of cells after said delaying.

76. The method of claim 75, wherein said determining includes:

averaging the phase of said current clock edges.